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(19) **United States**(12) **Patent Application Publication****Lee et al.**(10) **Pub. No.: US 2015/0035732 A1**(43) **Pub. Date: Feb. 5, 2015**(54) **STAGE AND ORGANIC LIGHT EMITTING
DISPLAY DEVICE USING THE SAME**(52) **U.S. CL.**CPC **G09G 3/3216** (2013.01); **G09G 2330/021**
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(57)

ABSTRACT(73) Assignee: **Samsung Display Co., Ltd.,**
Yongin-City (KR)(21) Appl. No.: **14/158,709**(22) Filed: **Jan. 17, 2014**(30) **Foreign Application Priority Data**

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(2006.01)

A stage includes an output unit configured to supply a scan signal to an output terminal according to voltages of first and second nodes; a first driver configured to control the voltages of the first and second nodes so that when a start signal or an output signal of a previous stage is supplied to a first input terminal, the scan signal is supplied from the output unit; and a second driver configured to control the voltages of the first and second nodes, corresponding to signals supplied to a second input terminal, a fourth input terminal and a fifth input terminal, wherein the second driver comprises eighth and ninth transistors coupled in series between the output terminal and the second node, and wherein a gate electrode of the eighth transistor is coupled to the first node, and a gate electrode of the ninth transistor is coupled to the fourth input terminal.

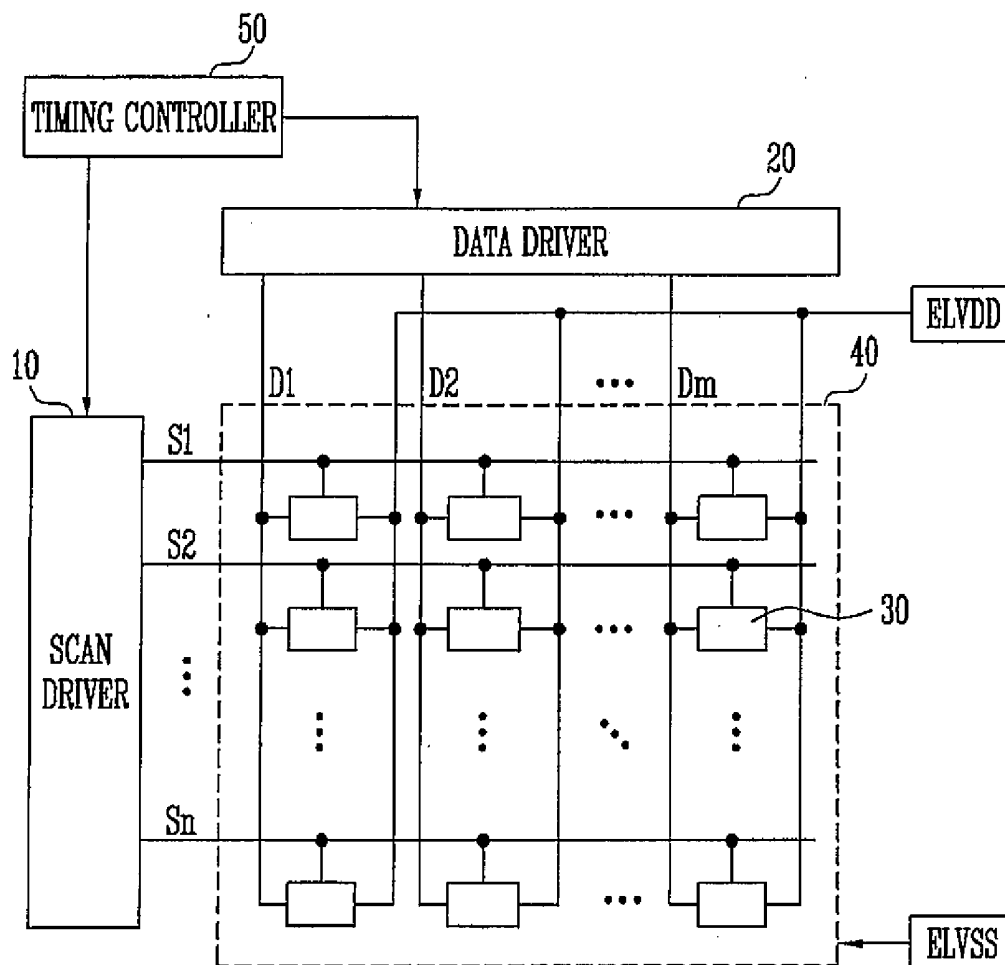


FIG. 1

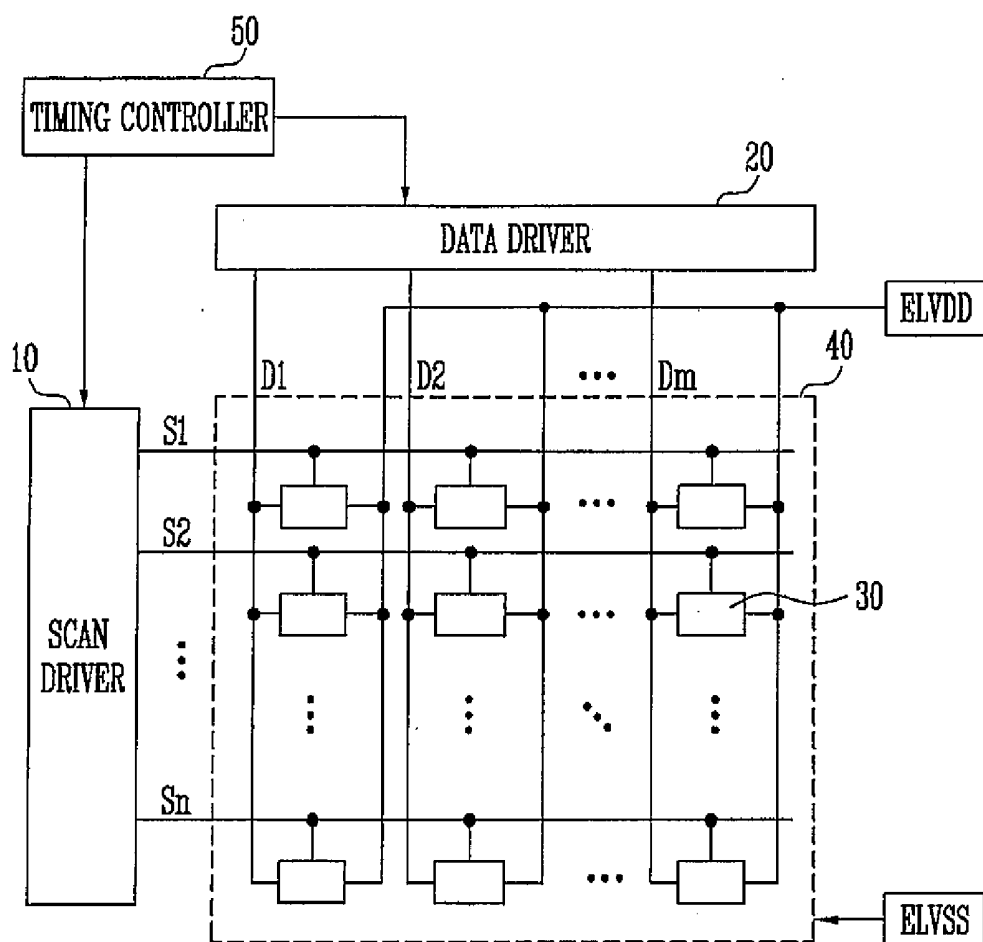


FIG. 2

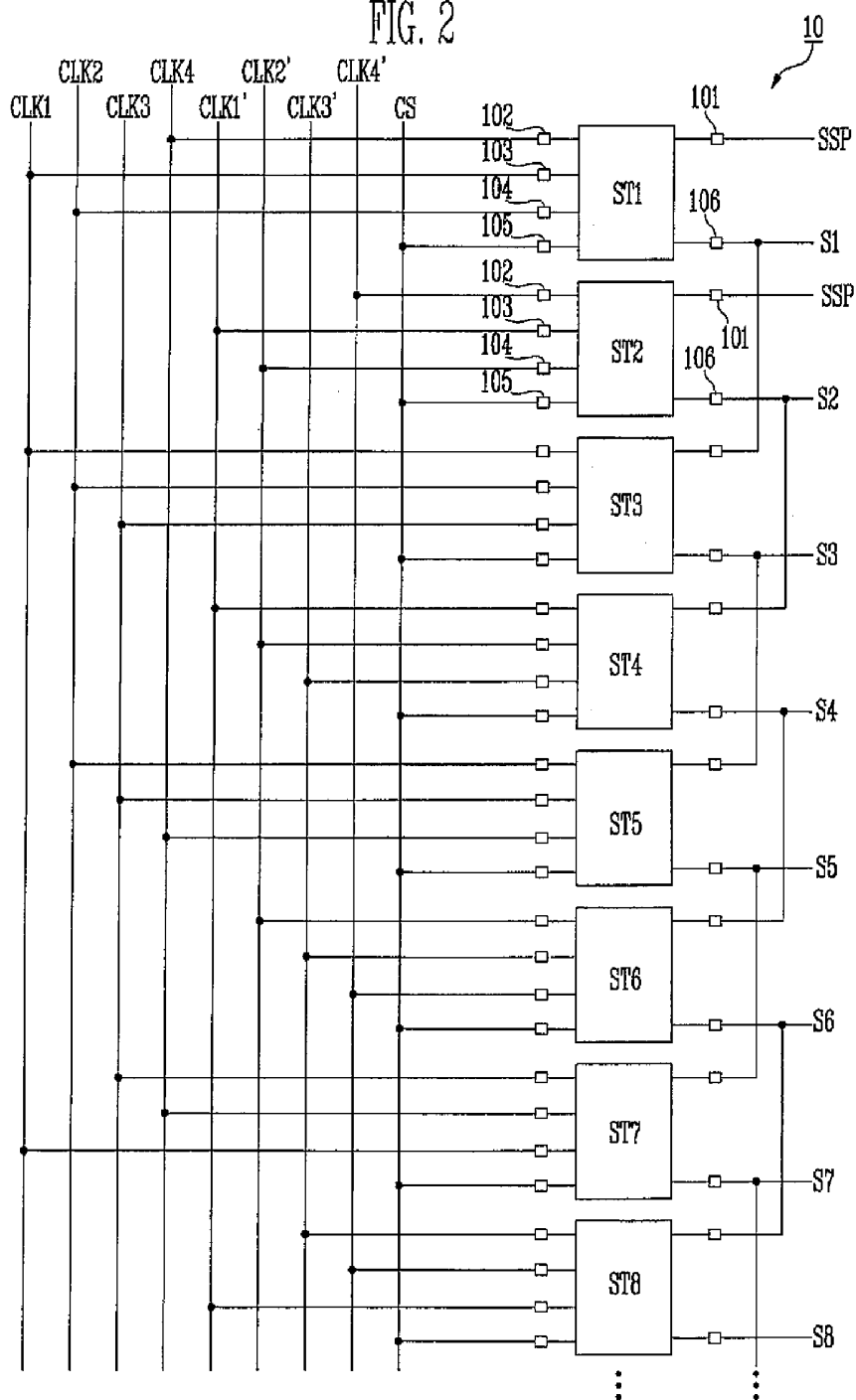


FIG. 3

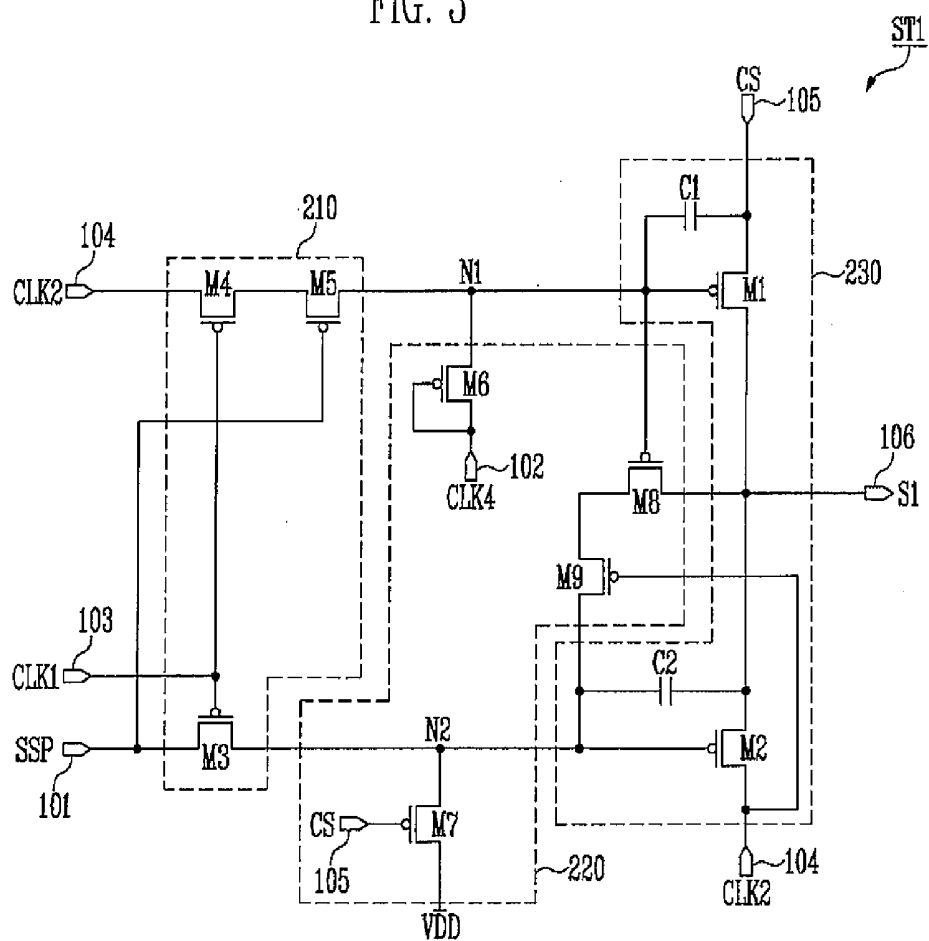


FIG. 4

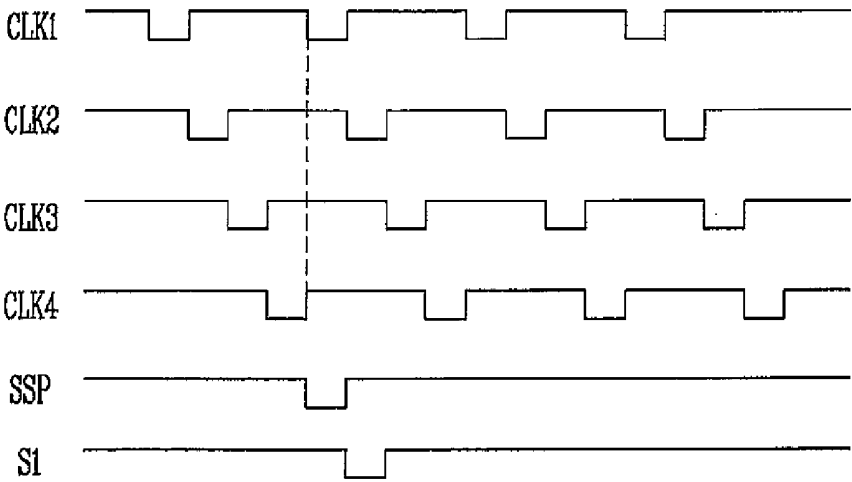


FIG. 5

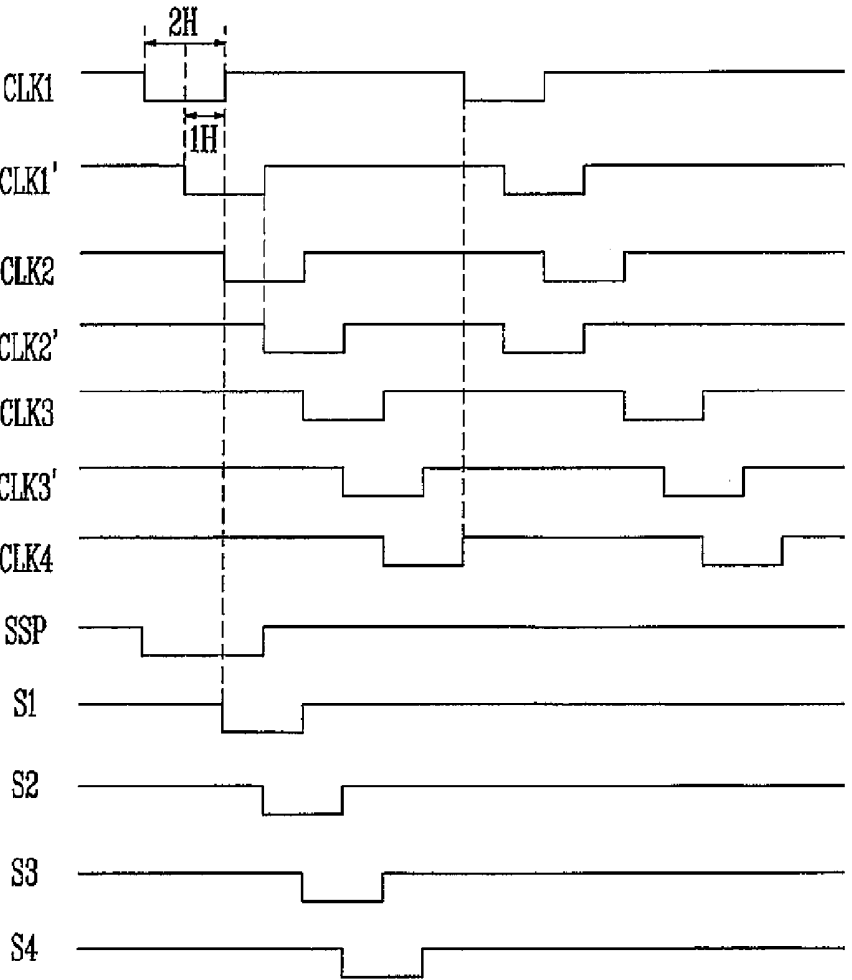


FIG. 6

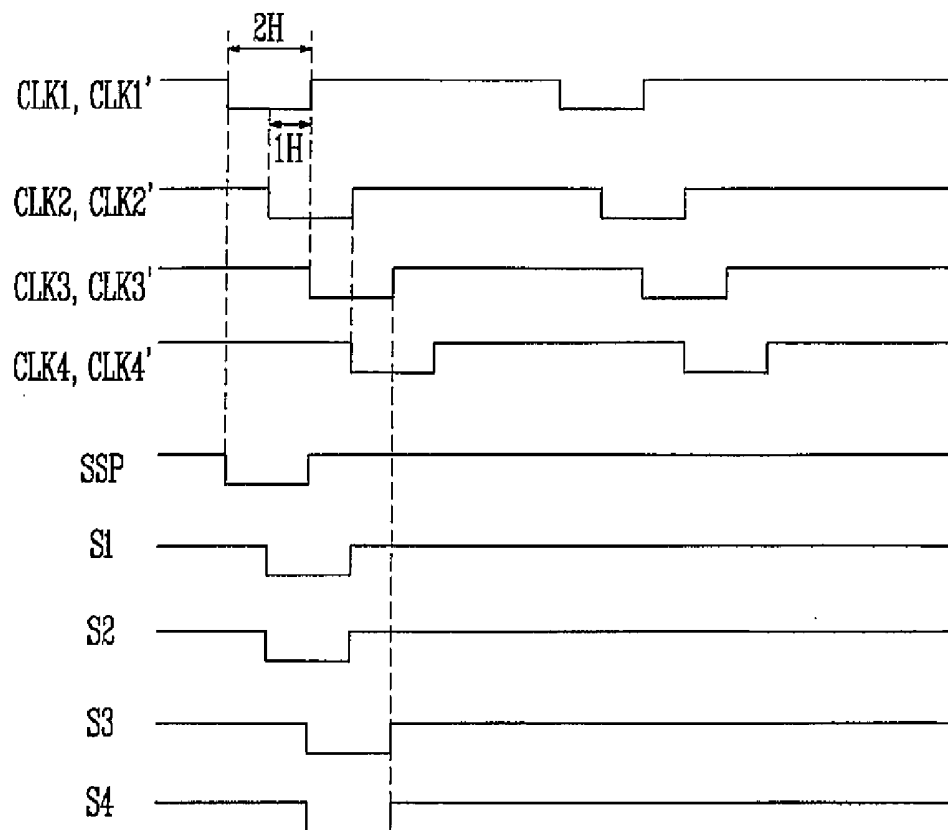


FIG. 7

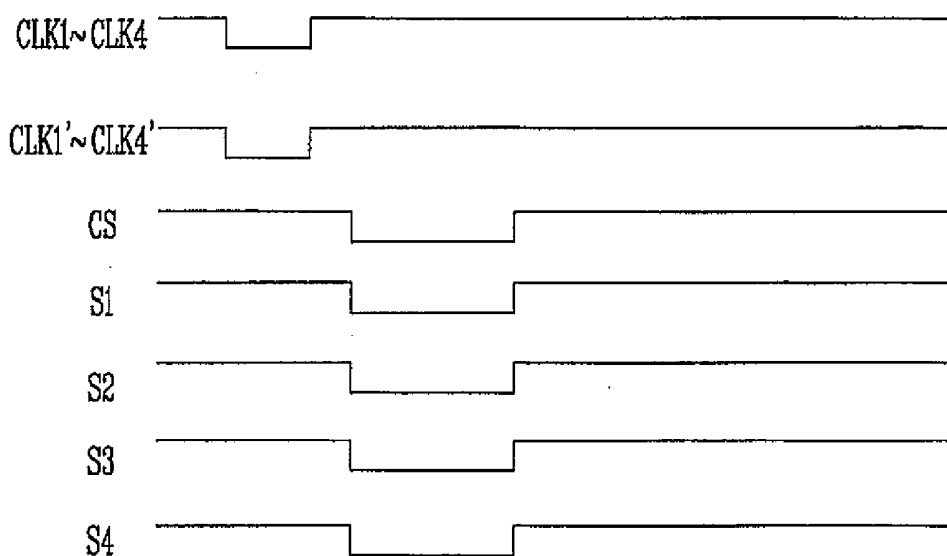


FIG. 8

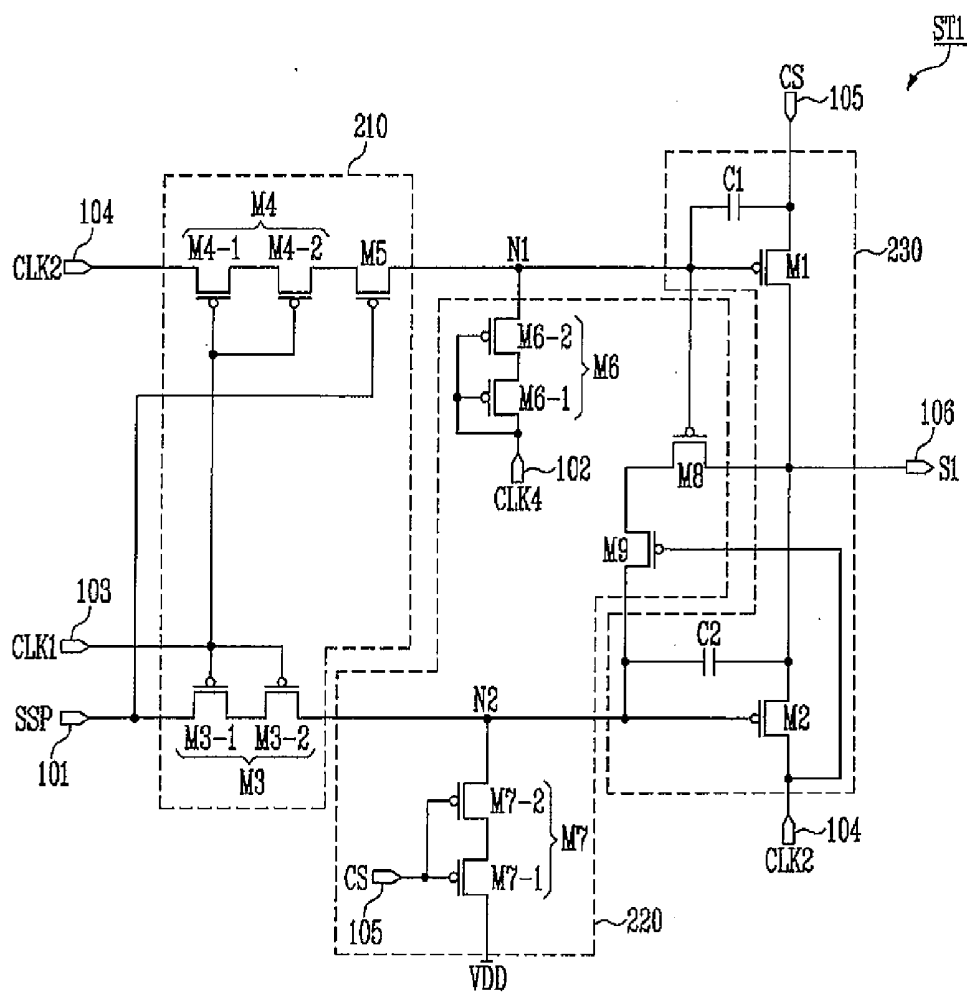
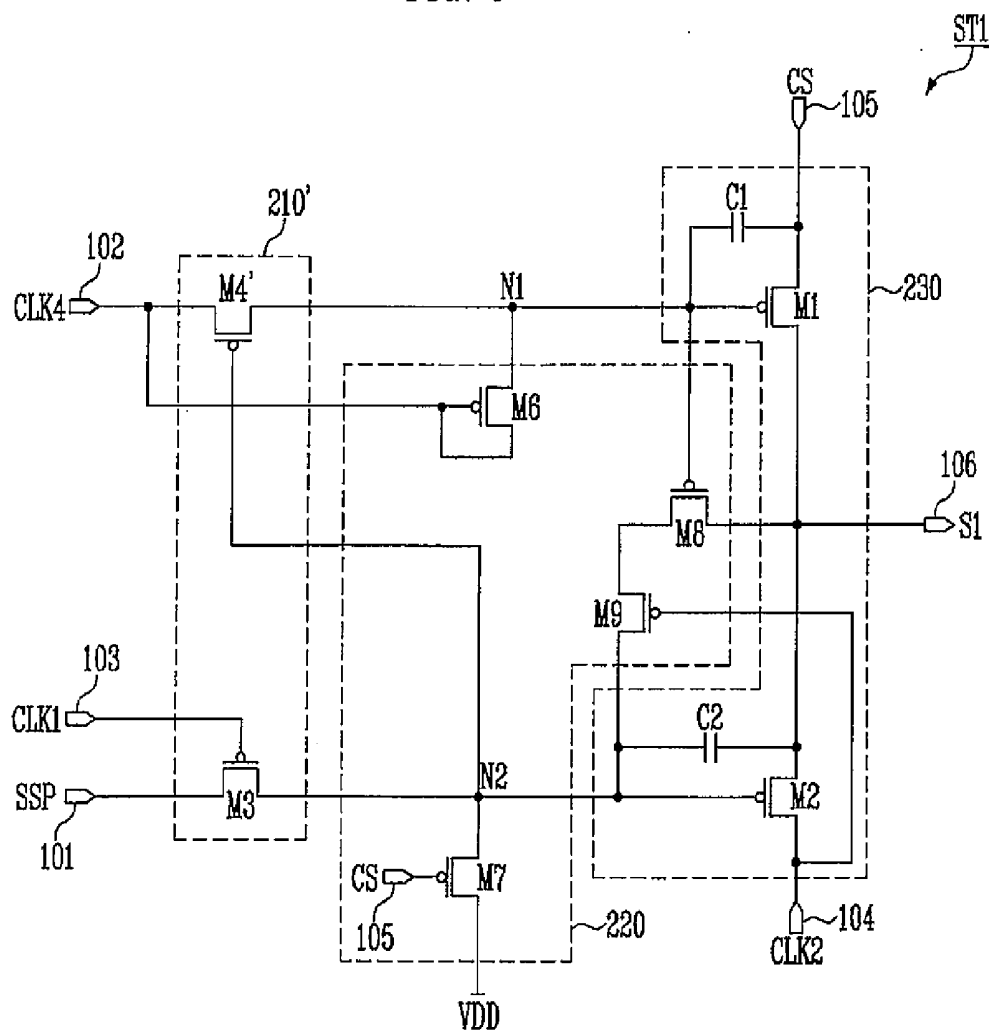


FIG. 9



STAGE AND ORGANIC LIGHT EMITTING DISPLAY DEVICE USING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2013-0091340, filed on Aug. 1, 2013, in the Korean Intellectual Property Office, the entire contents of which are incorporated herein by reference in their entirety.

BACKGROUND

[0002] 1. Field

[0003] Embodiments of the present invention relate to a stage and an organic light emitting diode display device using the same.

[0004] 2. Description of the Related Art

[0005] With the development of information technologies, the demand for display devices that operate as a connection medium for conveying information has increased. Accordingly, flat panel display devices (FPD devices) such as a liquid crystal display (LCD) device, an organic light emitting display device and a plasma display panel (PDP) are increasingly used.

[0006] Among these FPD devices, organic light emitting display devices display images using organic light emitting diodes (OLEDs) that emit light through recombination of electrons and holes. Organic light emitting display devices generally have a relatively fast response speed and are driven with relatively low power consumption, when compared with other types of FPD devices.

SUMMARY

[0007] Embodiments of the present invention provide a stage and an organic light emitting display device using the same, which are configured to supply scan signals in various orders.

[0008] According to an embodiment of the present invention, a stage includes: an output unit configured to supply a scan signal to an output terminal according to voltages of first and second nodes; a first driver configured to control the voltages of the first and second nodes so that when a start signal or an output signal of a previous stage is supplied to a first input terminal, the scan signal is supplied from the output unit; and a second driver configured to control the voltages of the first and second nodes, corresponding to signals supplied to a second input terminal, a fourth input terminal and a fifth input terminal, wherein the second driver includes eighth and ninth transistors coupled in series between the output terminal and the second node, and wherein a gate electrode of the eighth transistor is coupled to the first node, and a gate electrode of the ninth transistor is coupled to the fourth input terminal.

[0009] The output unit may include a first transistor between the fifth input terminal and the output terminal, the first transistor having a gate electrode coupled to the first node; a second transistor between the output terminal and the fourth input terminal, the second transistor having a gate electrode coupled to the second node; a first capacitor between the first node and the fifth input terminal; and a second capacitor between the second node and the output terminal.

[0010] The second driver may include a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second input terminal; and a seventh transistor between the second node and a first power source, the seventh transistor having a gate electrode coupled to the fifth input terminal.

[0011] The first power source may be set to a gate-off voltage.

[0012] Each of the sixth and seventh transistors may include a plurality of transistors coupled in series.

[0013] The first driver may include a third transistor between the first input terminal and the second node, the third transistor having a gate electrode coupled to a third input terminal; a fourth transistor between the fourth input terminal and the first node, the fourth transistor having a gate electrode coupled to the third input terminal; and a fifth transistor between the fourth transistor and the first node, the fifth transistor having a gate electrode coupled to the first input terminal.

[0014] Each of the third and fourth transistors may include a plurality of transistors coupled in series.

[0015] The first driver may include a third transistor between the first input terminal and the second node, the third transistor having a gate electrode coupled to a third input terminal; and a fourth transistor between the second input terminal and the first node, the fourth transistor having a gate electrode coupled to the second node.

[0016] According to an embodiment of the present invention, an organic light emitting diode display device includes: pixels in an area defined by scan lines and data lines; a data driver configured to supply data signals to the data lines; and a scan driver including stages respectively coupled to the scan lines so as to supply scan signals to the scan lines, wherein odd-numbered stages are configured to be driven by first signals and a control signal, and even-numbered stages are configured to be driven by second signals and the control signal.

[0017] Each stage may include a first input terminal configured to receive a start signal or an output signal of a previous stage; second, third, and fourth input terminals configured to receive the first or second signals; a fifth input terminal configured to receive the control signal; and an output terminal configured to output a corresponding one of the scan signals.

[0018] The first input terminals of a first stage and a second stage of the stages may be configured to receive the start signal.

[0019] The first input terminal of an odd-numbered stage of the stages may be configured to receive an output signal of a previous odd-numbered stage of the stages, and the first input terminal of an even-numbered stage of the stages may be configured to receive an output signal of a previous even-numbered stage of the stages.

[0020] Each of the first and second signals may include first, second, third, and fourth clock signals, and the first to fourth clock signals may be progressively supplied so that the voltage of the first to fourth clock signals are not overlapped at a low level with one another.

[0021] A k-th (k is 1, 2, 3 or 4) clock signal of the second signals may have a low level voltage that is overlapped with a low level voltage of a k-th clock signal of the first signals during at least one period.

[0022] The second, third, and fourth input terminals of an i-th (i is 1, 9, or a multiple of 9) stage and an (i+1)-th stage

may be configured to receive the fourth, first, and second clock signals, respectively, the second, third, and fourth input terminals of an (i+2)-th stage and an (i+3)-th stage may be configured to receive the first, second, and third clock signals, respectively, the second, third and fourth input terminals of an (i+4)-th stage and an (i+5)-th stage may be configured to receive the second, third, and fourth clock signals, respectively, and the second, third, and fourth input terminals of an (i+6)-th stage and an (i+7)-th stage may be configured to receive the third, fourth, and first clock signals, respectively.

[0023] Each stage may include an output unit configured to supply a corresponding one of the scan signals to the output terminal, according to voltages of first and second nodes; and first and second drivers configured to control the voltages of the first and second nodes.

[0024] The output unit may include a first transistor between the fifth input terminal and the output terminal, the first transistor having a gate electrode coupled to the first node; a second transistor between the output terminal and the fourth input terminal, the second transistor having a gate electrode coupled to the second node; a first capacitor between the first node and the fifth input terminal; and a second capacitor between the second node and the output terminal.

[0025] The first driver may include a third transistor between the first input terminal and the second node; the third transistor having a gate electrode coupled to a third input terminal; a fourth transistor between the fourth input terminal and the first node, the fourth transistor having a gate electrode coupled to the third input terminal; and a fifth transistor between the fourth transistor and the first node, the fifth transistor having a gate electrode coupled to the first input terminal.

[0026] The start signal or the output signal of the previous stage, supplied to the first input terminal, may be overlapped with a clock signal supplied to the third input terminal.

[0027] The first driver may include a third transistor between the first input terminal and the second node, the third transistor having a gate electrode coupled to the third input terminal; and a fourth transistor between the second input terminal and the first node, the fourth transistor having a gate electrode coupled to the second node.

[0028] The start signal or the output signal of the previous stage, supplied to the first input terminal, may be overlapped with a clock signal supplied to the third input terminal.

[0029] The second driver may include a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second input terminal; a seventh transistor between the second node and a first power source, the seventh transistor having a gate electrode coupled to the fifth input terminal; and eighth and ninth transistors coupled in series between the output terminal and the second node. A gate electrode of the eighth transistor may be coupled to the first node, and a gate electrode of the ninth transistor may be coupled to the fourth input terminal.

[0030] The first power source may be set to a gate-off voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031] Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings; however, they may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that

this disclosure will be thorough and complete, and will fully convey the scope of the example embodiments to those skilled in the art.

[0032] In the drawing figures, dimensions may be exaggerated for clarity of illustration. It will be understood that when an element is referred to as being “between” two elements, it can be the only element between the two elements, or one or more intervening elements may also be present. Like reference numerals refer to like elements throughout.

[0033] FIG. 1 is a diagram illustrating an organic light emitting display device according to an embodiment of the present invention.

[0034] FIG. 2 is a diagram illustrating an embodiment of stages included in a scan driver.

[0035] FIG. 3 is a circuit diagram illustrating an embodiment of the stage shown in FIG. 2.

[0036] FIG. 4 is a waveform diagram illustrating a driving method of the stage shown in FIG. 3.

[0037] FIG. 5 is a waveform diagram illustrating an embodiment in which a scan signal is output corresponding to the driving method of FIG. 4.

[0038] FIG. 6 is a waveform diagram illustrating another embodiment in which the scan signal is output corresponding to the driving method of FIG. 4.

[0039] FIG. 7 is a waveform diagram illustrating a driving waveform for concurrently (e.g., simultaneously) supplying a scan signal to scan lines.

[0040] FIG. 8 is a circuit diagram illustrating another embodiment of the stage shown in FIG. 2.

[0041] FIG. 9 is a circuit diagram illustrating still another embodiment of the stage shown in FIG. 2.

DETAILED DESCRIPTION

[0042] Hereinafter, certain example embodiments according to the present invention will be described with reference to the accompanying drawings. Here, when a first element is described as being coupled to a second element, the first element may be not only directly coupled to the second element, but may also be indirectly coupled to the second element via a third element. Further, some of the elements that are not essential to the complete understanding of the invention are omitted for clarity. Also, like reference numerals refer to like elements throughout.

[0043] FIG. 1 is a diagram illustrating an organic light emitting display device according to an embodiment of the present invention.

[0044] Referring to FIG. 1, the organic light emitting display device according to this embodiment includes a pixel unit 40 including pixels 30 positioned at intersection portions of scan lines S1 to Sn and data lines D1 to Dm, a scan driver 10 configured to drive the scan lines S1 to Sn, a data driver 20 configured to drive data lines D1 to Dm, and a timing controller 50 configured to control the scan driver 10 and the data driver 20.

[0045] The scan driver 10 supplies scan signals to the scan lines S1 to Sn. The scan driver 10 may concurrently (e.g., simultaneously) or progressively supply the scan signal to the scan lines S1 to Sn. The scan driver 10 may supply scan signals to odd-numbered scan lines (e.g., S1, S3, . . .) and even-numbered scan lines (e.g., S2, S4, . . .) during different periods. To this end, the scan driver 10 may include stages (shown, e.g., in FIG. 2) respectively coupled to the scan lines S1 to Sn.

[0046] The data driver 20 supplies a data signal to the data lines D1 to Dm to be synchronized with the scan signal.

[0047] The timing controller 50 supplies control signals (not shown) for controlling the scan driver 10 and the data driver 20. The timing controller 50 supplies data (not shown) from the outside of the organic light emitting display device to the data driver 20.

[0048] The pixels 30 are selected when the scan signal is supplied, to charge a voltage corresponding to the data signal. Each of the selected pixels 30 generates light with a luminance (e.g., a predetermined luminance) while supplying, to an organic light emitting diode (not shown), current corresponding to the charged voltage.

[0049] FIG. 2 is a diagram illustrating an embodiment of stages included in a scan driver. For convenience of illustration, eight stages will be shown in FIG. 2, although the number of stages may vary according to the design and structure of the organic light emitting display device.

[0050] Referring to FIG. 2, the scan driver 10 according to this embodiment includes stages ST1 to ST8 respectively coupled to scan lines S1 to S8. Each of the stages ST1 to ST8 is coupled to any one of the scan lines S1 to S8. The stages ST1 to ST8 may be configured with the same circuit.

[0051] Odd-numbered (or even-numbered) stages (e.g., ST1, ST3, . . .) are driven by first signals CLK1 to CLK4 and a control signal CS, and even-numbered (or odd-numbered) stages (e.g., S2, S4, . . .) are driven by second signals CLK1' to CLK4' and the control signal CS. To this end, each of the stages ST1 to ST8 includes first to fifth input terminals 101 to 105 and an output terminal 106.

[0052] The first input terminal 101 included in each of the stages ST1 to ST8 receives a start signal SSP or an output signal (e.g., a scan signal) of the previous stage. For example, the first input terminals 101 of the first and second stages ST1 and ST2 receive the start signal SSP. Here, the start signal SSP is supplied to overlap with clock signals respectively supplied to the third input terminals 103 of the first and second stages ST1 and ST2. The first input terminal 101 of the odd-numbered (or even-numbered) stage receives a scan signal of the previous odd-numbered (or even-numbered) stage.

[0053] The second, third, and fourth input terminals 102, 103, and 104 of an i-th (i is 1, 9, or a multiple of 9) receive a fourth clock signal CLK4, a first clock signal CLK1, and a second clock signals CLK2, respectively.

[0054] The second, third, and fourth input terminals 102, 103, and 104 of an (i+1)-th stage receive a fourth clock signal CLK4', a first clock signal CLK', and a second clock signal CLK2', respectively.

[0055] The second, third, and fourth input terminals 102, 103 and 104 of an (i+2)-th stage receive the first clock signal CLK1, the second clock signal CLK2, and a third clock signal CLK3, respectively.

[0056] The second, third and fourth input terminals 102, 103, and 104 of an (i+3)-th stage receive the first clock signal CLK1', the second clock signal CLK2', and a third clock signal CLK3', respectively.

[0057] The second, third and fourth input terminals 102, 103, and 104 of an (i+4)-th stage receive the second clock signal CLK2, the third clock signal CLK3, and the fourth clock signal CLK4, respectively.

[0058] The second, third and fourth input terminals 102, 103, and 104 of an (i+5)-th stage receive the second clock signal CLK2', the third clock signal CLK3', and the fourth clock signal CLK4', respectively.

[0059] The second, third and fourth input terminals 102, 103, and 104 of an (i+6)-th stage receive the third clock signal CLK3, the fourth clock signal CLK4, and the first clock signal CLK1, respectively.

[0060] The second, third and fourth input terminals 102, 103, and 104 of an (i+7)-th stage receive the third clock signal CLK3', the fourth clock signal CLK4', and the first clock signal CLK1', respectively.

[0061] The first to fourth clock signals CLK1 to CLK4 included in the first signal are progressively supplied so that the phases of the first to fourth clock signals CLK1 to CLK4 are not overlapped with one another (i.e., so that the low levels of the first to fourth clock signals CLK1 to CLK4 are not overlapped with one another). For example, each of the first to fourth clock signals CLK1 to CLK4 may have a low level during a period of 2H. The first to fourth clock signals CLK1 to CLK4 may be progressively supplied so that the low levels of the first to fourth clock signals CLK1 to CLK4 are not overlapped with one another.

[0062] Similarly, the first to fourth clock signals CLK1' to CLK4' included in the second signal are progressively supplied so that the phases of the first to fourth clock signals CLK1' to CLK4' are not overlapped with one another. For example, each of the first to fourth clock signals CLK1' to CLK4' may have a low level during a period of 2H. The first to fourth clock signals CLK1' to CLK4' may be progressively supplied so that the low levels of the first to fourth clock signals CLK1' to CLK4' are not overlapped with one another. A k-th (k is 1, 2, 3, or 4) clock signal CLKk' included in the second signal may be supplied so that the low level of the k-th clock signal CLKk' is overlapped with that of a k-th clock signal CLKk included in the first signal during at least one period (e.g., a period of 1H).

[0063] FIG. 3 is a circuit diagram illustrating an example embodiment of one of the stages shown in FIG. 2. For convenience of illustration, the first stage ST1 will be shown in FIG. 3.

[0064] Referring to FIG. 3, the stage ST1 according to this embodiment includes a first driver 210, a second driver 220, and an output unit 230.

[0065] The output unit 230 controls a voltage supplied to the output terminal 106, corresponding to voltages of the first and second nodes N1 and N2. To this end, the output unit 230 includes a first transistor M1, a second transistor M2, a first capacitor C1, and a second capacitor C1.

[0066] The first transistor M1 is positioned between the fifth input terminal 105 and the output terminal 106. A gate electrode of the first transistor M1 is coupled to the first node N1. The first transistor M1 controls the coupling between the fifth input terminal 105 and the output terminal 106, corresponding to the voltage of the first node N1. Here, the fifth input terminal 105 is a terminal which receives a control signal CS, and maintains a high voltage (gate-off voltage) during a period in which the control signal CS is not supplied.

[0067] The second transistor M2 is positioned between the output terminal 106 and the fourth input terminal 104. A gate electrode of the second transistor M2 is coupled to the second node N2. The second transistor M2 controls the coupling between the output terminal 106 and the fourth input terminal 104, corresponding to the voltage of the second node N2.

[0068] The first capacitor C1 is coupled between the first node N1 and the fifth input terminal 105. The first capacitor C1 charges a voltage corresponding to the turn-on or turn-off of the first transistor M1.

[0069] The second capacitor C2 is coupled between the second node N2 and the output terminal 106. The second capacitor C2 charges a voltage corresponding to the turn-on or turn-off of the second transistor M2.

[0070] The first driver 210 controls the voltages of the first and second nodes N1 and N2, corresponding to signals supplied to the first, third and fourth input terminals 101, 103, and 104. For example, the first driver 210 controls the voltages of the first and second nodes N1 and N2 so that the scan signal can be supplied from the output unit 230 when the output signal (e.g., the scan signal) of the previous stage is input.

[0071] To this end, the first driver 210 includes a third transistor M3, a fourth transistor M4, and a fifth transistor M5.

[0072] The third transistor M3 is positioned between the first input terminal 101 and the second node N2. A gate electrode of the third transistor M3 is coupled to the third input terminal 103. The third transistor M3 is turned on when the first clock signal CLK1 is supplied to the third terminal 103, to allow the first input terminal 101 and the second node N2 to be electrically coupled to each other.

[0073] The fourth transistor M4 is positioned between the fourth input terminal 104 and the fifth transistor M5 (or the first node N1). A gate electrode of the fourth transistor M4 is coupled to the third input terminal. The fourth transistor M4 is turned on when the clock signal CLK1 is supplied to the third input terminal 103, to allow the fourth input terminal 104 and the fifth transistor M5 to be electrically coupled to each other.

[0074] The fifth transistor M5 is positioned between the fourth transistor M4 and the first node N1. A gate electrode of the fifth transistor M5 is coupled to the first input terminal 101. The fifth transistor M5 allows the fourth transistor M4 and the first node N1 to be electrically coupled to each other when the start signal SSP or the output signal of the previous stage is input to the first input terminal 101.

[0075] The second driver 220 controls the voltages of the first and second nodes N1 and N2, corresponding to signals supplied to the second, fourth and fifth input terminals 102, 104, and 105. To this end, the second driver 220 includes a sixth transistor M6, a seventh transistor M7, an eighth transistor M8, and a ninth transistor M9.

[0076] The sixth transistor M6 is positioned between the first node N1 and the second input terminal 102. A gate electrode of the sixth transistor M6 is coupled to the second input terminal 102. That is, the sixth transistor M6 is diode-coupled. The sixth transistor M6 is turned on when the clock signal CLK4 is supplied to the second input terminal 102.

[0077] The seventh transistor M7 is positioned between the second node N2 and a first power source VDD. A gate electrode of the seventh transistor M7 is coupled to the fifth input terminal 105. The seventh transistor M7 is turned on when the control signal CS is supplied to the fifth input terminal 105, to supply the voltage of the first power source VDD to the second node N2. Here, the first power source VDD is set to a high voltage (e.g., a data-off voltage).

[0078] The eighth and ninth transistors M8 and M9 are coupled in series between the output terminal 106 and the second node N2. A gate electrode of the eighth transistor M8 is coupled to the first node N1, and a gate electrode of the ninth transistor M9 is coupled to the fourth input terminal 104. The eighth transistor M8 controls the electrical coupling between the output terminal 106 and the ninth transistor M9, corresponding to the voltage of the first node N1. The ninth

transistor M9 controls the electrical coupling between the eighth transistor M8 and the second node N2, corresponding to the clock signal CLK2 supplied to the fourth input terminal 104.

[0079] FIG. 4 is a waveform diagram illustrating a driving method of the stage shown in FIG. 3.

[0080] Referring to FIG. 4, the clock signals CLK1 to CLK4 are progressively supplied such that the low levels of the clock signals CLK1 to CLK4 are not overlapped with one another. The start signal SSP is supplied to the first input terminal 101 to overlap with the first clock signal CLK1 supplied to the third input terminal 103.

[0081] If the first clock signal CLK1 is supplied to the third input terminal 103, the third and fourth transistors M3 and M4 are turned on. If the start signal SSP is supplied to the first input terminal 101, the fifth transistor M5 is turned on.

[0082] If the third transistor M3 is turned on, the first input terminal 101 and the second node N2 are electrically coupled to each other. In this case, the second node N2 is set to a low voltage by the start signal SSP supplied to the first input terminal 101. If the second node N2 is set to the low voltage, the second transistor M2 is turned on.

[0083] If the second transistor M2 is turned on, the output terminal 106 and the second input terminal 104 are electrically coupled to each other. In this case, the fourth input terminal 104 is set to a high voltage (i.e., the second clock signal CLK2 is not supplied), and accordingly, the high voltage is also output to the output terminal 106 (i.e., the scan signal is not supplied).

[0084] Meanwhile, if the fourth and fifth transistors M4 and M5 are turned on, the fourth input terminal 104 and the first node N1 are electrically coupled to each other. In this case, the first node N1 receives the high voltage supplied from the fourth input terminal 104, and accordingly, the first transistor M1 is set to a turn-off state.

[0085] Subsequently, the second clock signal CLK2 is supplied to the fourth input terminal 104. In this case, the second transistor M2 is set to a turn-on state, corresponding to a voltage of the second capacitor C2, and hence the second clock signal CLK2 supplied to the fourth input terminal 104 is supplied to the output terminal 106. When the second clock signal CLK2 is supplied to the output terminal 106, the voltage of the second node N2 is dropped to a voltage lower than that of the second clock signal CLK2 by the coupling of the second capacitor C2, and accordingly, the second transistor M2 stably maintains the turn-on state. The second clock signal CLK2 supplied to the output terminal 106 is output as a scan signal to the scan line S1.

[0086] Meanwhile, if the second clock signal CLK2 is supplied to the fourth input terminal 104, the ninth transistor M9 is turned on. In this case, the eighth transistor M8 is set to the turn-off state, corresponding to the high voltage applied to the first node N1, and hence the second node N2 stably maintains the low voltage even though the ninth transistor M9 is turned on. Since the fourth transistor M4 is set to the turn-off state during the period in which the second clock signal CLK2 is supplied to the fourth input terminal 104, the voltage of the second clock signal CLK2 is not supplied to the first node N1. After the scan signal is supplied to the output terminal 106, the fourth clock signal CLK4 is supplied to the second input terminal 102. If the fourth clock signal CLK4 is supplied to the second input terminal 102, the sixth transistor M6 is turned on. If the sixth transistor M6 is turned on, the first node N1 is dropped to a low voltage by the fourth clock signal

CLK4. If the first node N1 is set to the low voltage, the first transistor M1 is turned on. If the first transistor M1 is turned on, the high voltage from the fifth input terminal 105 is supplied to the output terminal 106.

[0087] Subsequently, the first clock signal CLK1 is supplied to the third input terminal 103 so that the third transistor M3 is turned on. If the third transistor M3 is turned on, the first input terminal 101 and the second node N2 are electrically coupled to each other. In this case, the start signal SSP is not supplied to the first input terminal 101, and hence the second node N2 is raised to the high voltage. If the second node N2 is set to the high voltage, the second transistor M2 is turned off.

[0088] Subsequently, the second clock signal CLK2 is supplied to the fourth input terminal 104 so that the ninth transistor M9 is turned on. In this case, the eighth transistor M8 is set to the turn-on state, corresponding to the voltage of the first node N1, and hence the output terminal 106 and the second node N2 are electrically coupled to each other, corresponding to the turn-on of the ninth transistor M9. In this case, the second node N2 receives the high voltage.

[0089] According to embodiments of the present invention, the scan signal is output to the output terminal 106 by repeating the aforementioned process. Whenever the fourth clock signal CLK4 is supplied during the period in which the scan signal is not output, the first node N1 is set to the low voltage, and the second node N2 is set to the high voltage, using the second clock signal CLK2. Then, the first and second nodes N1 and N2 are set to a voltage (e.g., a desired voltage), to improve reliability.

[0090] FIG. 5 is a waveform diagram illustrating an embodiment in which a scan signal is output corresponding to the driving method of FIG. 4.

[0091] Referring to FIG. 5, the clock signals CLK1 to CLK4 included in the first signal are set to the voltage of the low level during two horizontal periods 2H. The clock signals CLK1 to CLK4 are sequentially supplied so that the voltages of the low levels of the clock signals CLK1 to CLK4 are not overlapped with one another. Similarly, the clock signals CLK1' to CLK4' included in the second signal are set to the voltage of the low level during two horizontal periods 2H. The clock signals CLK1' to CLK4' are sequentially supplied such that the voltages of the low levels of the clock signals CLK1' to CLK4' are not overlapped with one another. The k-th clock signal CLKk' included in the second signal is set so that the low level of the k-th clock signal

[0092] CLKk' is overlapped with that of the k-th clock signal CLKk included in the first signal during one horizontal period 1H.

[0093] The start signal SSP is supplied to overlap with the first clock signal CLK1 supplied to the third input terminal 103 of the first stage ST1 and the first clock signal CLK1' supplied to the third input terminal of the second stage ST2.

[0094] In this case, the first stage ST1 outputs, to the first scan line S1, the second clock signal CLK2 supplied to the fourth input terminal 104 as a scan signal. The second stage ST2 outputs, to the second scan line S2, the second clock signal CLK2' supplied to the fourth input terminal 104 as a scan signal. The third stage ST3 outputs, to the third scan line S3, the third clock signal CLK3 supplied to the fourth input terminal 104 as a scan signal. The fourth stage ST4 outputs, to the fourth scan line S4, the third clock signal CLK3' supplied to the fourth input terminal 104 as a scan signal.

[0095] According to embodiments of the present invention, the scan signal can be supplied to the current scan line to

overlap with the previous scan signal during a partial period while repeating the aforementioned process. Further, the clock signals CLK1' to CLK4' included in the second signal can be supplied to not overlap with the clock signals CLK1 to CLK4 including in the first signal. Then, the scan signal is progressively output so that the current scan signal is not overlapped with the previous scan signal.

[0096] As described above, according to embodiments of the present invention, the scan signal can be output in various manners while controlling the overlapping, width and the like of the clock signals CLK1 to CLK4 and CLK1' to CLK4'.

[0097] FIG. 6 is a waveform diagram illustrating another embodiment in which the scan signal is output corresponding to the driving method of FIG. 4.

[0098] Referring to FIG. 6, the clock signals CLK1 to CLK4 included in the first signal are set to the voltage of the low level during two horizontal periods 2H. The clock signals CLK1 to CLK4 are progressively supplied so that the voltage of the low level of the previous clock signal is overlapped with that of the current clock signal during one horizontal period 1H. Similarly, the clock signals CLK1' to CLK4' included in the second signal are set to the voltage of the low level during two horizontal periods 2H. The clock signals CLK1' to CLK4' are progressively supplied so that the voltage of the low level of the previous clock signal is overlapped with that of the current clock signal during one horizontal period 1H. The k-th clock signal CLKk' included in the second signal is set so that the low level of the k-th clock signal CLKk' is overlapped with that of the k-th clock signal CLKk included in the first signal.

[0099] Then, the first and second stages ST1 and ST2 concurrently (e.g., simultaneously) supply a scan signal to the first and second scan lines S1 to Sn. Similarly, the third and fourth stages ST3 and ST4 concurrently (e.g., simultaneously) supply a scan signal to the third and fourth scan lines S3 and S4. Here, the scan signal supplied to the third scan line S3 is overlapped with that supplied to the first scan line S1 during a partial period (1H).

[0100] FIG. 7 is a waveform diagram illustrating a driving waveform for concurrently (e.g., simultaneously) supplying a scan signal to the scan lines.

[0101] The operating process of the stage will be described in conjunction with FIGS. 3 and 7. First, the clock signals CLK1 to CLK4 and CLK1' to CLK4' are concurrently (e.g., simultaneously) supplied. Then, the first node N1 is set to the low voltage, corresponding to the clock signal CLK4 supplied to the second input terminal 102. If the first node N1 is set to the low voltage, the first transistor M1 is turned on so that the output terminal 106 and the fifth input terminal 105 are electrically coupled to each other.

[0102] Subsequently, the control signal CS is supplied to the fifth input terminal 105. If the control signal CS is supplied to the fifth input terminal 105, the control signal CS is output to the output terminal 106. The output terminal 106 supplies, to the scan line S1, the control signal CS as a scan signal. Here, the control signal CS is commonly coupled to the fifth input terminals 105 of all the stages, and accordingly, the scan signal is concurrently (e.g., simultaneously) supplied to the scan lines S1 to Sn.

[0103] Meanwhile, when the control signal CS is supplied to the fifth input terminal 105, the voltage of the first node N1 is additionally dropped by the coupling of the first capacitor

C1. Thus, the first transistor M1 stably maintains the turn-on state during the period in which the control signal CS is supplied.

[0104] If the control signal CS is supplied to the fifth input terminal 105, the seventh transistor M7 is turned on. If the seventh transistor M7 is turned on, the voltage of the first power source VDD is supplied to the second node N2. If the voltage of the first power source VDD is supplied to the second node N2, the second transistor M2 is set to the turn-off state.

[0105] FIG. 8 is a circuit diagram illustrating another embodiment of the stage shown in FIG. 2. In, FIG. 8, components identical to those of FIG. 3 are designated by like reference numerals, and their detailed descriptions will be omitted.

[0106] Referring to FIG. 8, in this embodiment, each of the third, fourth, sixth, and seventh transistors M3, M4, M6, and M7 shown in FIG. 3 is configured with a plurality of transistors, and accordingly, it is possible to minimize leakage current.

[0107] More specifically, the third transistors M3 is configured with a plurality of transistors M3-1 and M3-2 coupled in series between the first input terminal 101 and the second node N2. Gate electrodes of the third transistors M3-1 and M3-2 are coupled to the third input terminal 103.

[0108] The fourth transistor M4 is configured with a plurality of transistors M4-1 and M4-2 coupled in series between the fourth input terminal 104 and the fifth transistor M5. Gate electrodes of the fourth transistors M4-1 and M4-2 are coupled to the third input terminal 103.

[0109] The sixth transistor M6 is configured with a plurality of transistors M6-1 and M6-2 coupled in series between the first node N1 and the second input terminal 102. Gate electrodes of the sixth transistors M6-1 and M6-2 are coupled to the second input terminal 102.

[0110] The seventh transistor M7 is configured with a plurality of transistors M7-1 and M7-2 coupled in series between the second node N2 and the first power source VDD. Gate electrodes of the seventh transistors M7-1 and M7-2 are coupled to the fifth input terminal 105.

[0111] The operating process of the stage according to this embodiment configured as described above is similar or substantially identical to that of the stage of FIG. 3, except that each of the third, fourth, sixth, and seventh transistors M3, M4, M6, and M7 is configured with a plurality of transistors. Therefore, its detailed description will be omitted.

[0112] FIG. 9 is a circuit diagram illustrating still another embodiment of the stage shown in FIG. 2. In FIG. 9, components identical to those of FIG. 3 are designated by like reference numerals, and their detailed descriptions will be omitted.

[0113] Referring to FIG. 9, the stage ST1 according to this embodiment includes a first driver 210', the second driver 220 and an output unit 230. When comparing this embodiment with the embodiment of FIG. 3, the fifth transistor M5 is removed, and the coupling configuration of the fourth transistor M4 is changed.

[0114] A fourth transistor M4' included in the first driver 210' is positioned between the second input terminal 102 and the first node N1. A gate electrode of the fourth transistor M4' is coupled to the second node N2. The fourth transistor M4' controls the electrical coupling between the second input terminal 102 and the first node N1, corresponding to the voltage of the second node N2.

[0115] The operating process of the stage will be described in conjunction with FIGS. 4 and 9. First, the start signal SSP is supplied to the first input terminal 101 to overlap with the first clock signal CLK1 supplied to the third input terminal 103.

[0116] If the first clock signal CLK1 is supplied to the third input terminal 103, the third transistor M3 is turned on. If the third transistor M3 is turned on, the first input terminal 101 and the second node N2 are electrically coupled to each other. In this case, the second node N2 is set to the low voltage by the start signal SSP supplied to the first input terminal 101. If the second node N2 is set to the low voltage, the second and fourth transistors M2 and M4' are turned on.

[0117] If the second transistor M2 is turned on, the output terminal 106 and the fourth input terminal 104 are electrically coupled to each other. In this case, the fourth input terminal 104 is set to the high voltage, and accordingly, the high voltage is also output to the output terminal 106 (i.e., the scan signal is not supplied).

[0118] If the fourth transistor M4' is turned on, the high voltage of the fourth input terminal 104 is supplied to the first node N1. If the first node N1 is set to the high voltage, the first transistor M1 is turned off.

[0119] Subsequently, the second clock signal CLK2 is supplied to the fourth input terminal 104. The second clock signal CLK2 supplied to the fourth input terminal 104 is supplied to the output terminal 106 via the second transistor M2. The second clock signal CLK2 supplied to the output terminal 106 is output as a scan signal to the scan line S1.

[0120] Meanwhile, if the second clock signal CLK2 is supplied to the fourth input terminal 104, the ninth transistor M9 is turned on. In this case, the eighth transistor M8 is set to the turn-off state, corresponding to the high voltage applied to the first node N1, and hence the second node N2 stably maintains the low voltage even though the ninth transistor M9 is turned on.

[0121] After the scan signal is supplied to the output terminal 106, the fourth clock signal CLK4 is supplied to the second input terminal 102. If the fourth clock signal CLK4 is supplied to the second input terminal 102, the sixth transistor M6 is turned on. If the sixth transistor M6 is turned on, the first node N1 is dropped to the low voltage by the fourth clock signal CLK4. If the first node N1 is set to the low voltage, the first transistor M1 is turned on. If the first transistor M1 is turned on, the high voltage from the fifth input terminal 105 is supplied to the output terminal 106.

[0122] Subsequently, the first clock signal CLK1 is supplied to the third input terminal 103 so that the third transistor M3 is turned on. If the third transistor M3 is turned on, the first input terminal 101 and the second node N2 are electrically coupled to each other. In this case, the start signal SSP is not supplied to the first input terminal 101, and hence the second node N2 is raised to the high voltage. If the second node N2 is set to the high voltage, the second and fourth transistors M2 and M4' are turned off.

[0123] Subsequently, the second clock signal CLK2 is supplied to the fourth input terminal 104 so that the ninth transistor M9 is turned on. In this case, the eighth transistor M8 is set to the turn-on state, corresponding to the voltage of the first node N1, and hence the output terminal 106 and the second node N2 are electrically coupled to each other, corresponding to the turn-on of the ninth transistor M9. Here, the second node N2 receives the high voltage.

[0124] According to embodiments of the present invention, the scan signal is output to the output terminal 106 while repeating the aforementioned process.

[0125] Meanwhile, although it has been described with respect to example embodiments of the present invention that the transistors are shown as PMOS transistors for convenience of illustration, the present invention is not limited thereto. In other words, the transistors may be formed as NMOS transistors.

[0126] By way of summation and review, an organic light emitting display device includes a data driver configured to supply a data signal to data lines, a scan driver configured to progressively supply a scan signal to scan lines, and a pixel unit configured to include a plurality of pixels coupled to the scan lines and the data lines.

[0127] Pixels included in the pixel unit are selected when a scan signal is supplied to a scan line, to receive a data signal from a data line. The pixels receiving the data signal generate light with a luminance (e.g., a predetermined luminance) corresponding to the data signal, thereby displaying an image.

[0128] The organic light emitting display device is driven by various driving methods including a 3D driving method. For example, the organic light emitting display device may be driven by a dual view method in which observers each wearing shutter glasses view different images, using a fast response speed. Thus, a scan driver capable of supplying a scan signal is required to be applicable to various driving methods.

[0129] In the stage and the organic light emitting display device using the same according to embodiments of the present invention, scan signals can be supplied in various orders by controlling clock signals. That is, according to embodiments of the present invention, the scan signals can be progressively supplied or may be supplied to overlap with the previous scan signal during a period (e.g., a predetermined period). Further, the scan signal can be concurrently (e.g., simultaneously) supplied.

[0130] Example embodiments have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. In some instances, as would be apparent to one of ordinary skill in the art as of the filing of the present application, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise specifically indicated. Accordingly, it will be understood by those of skill in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims, and their equivalents.

What is claimed is:

1. A stage comprising:

an output unit configured to supply a scan signal to an output terminal according to voltages of first and second nodes;

a first driver configured to control the voltages of the first and second nodes so that when a start signal or an output signal of a previous stage is supplied to a first input terminal, the scan signal is supplied from the output unit; and

a second driver configured to control the voltages of the first and second nodes, corresponding to signals supplied to a second input terminal, a fourth input terminal and a fifth input terminal,

wherein the second driver comprises eighth and ninth transistors coupled in series between the output terminal and the second node, and

wherein a gate electrode of the eighth transistor is coupled to the first node, and a gate electrode of the ninth transistor is coupled to the fourth input terminal.

2. The stage of claim 1, wherein the output unit comprises: a first transistor between the fifth input terminal and the output terminal, the first transistor having a gate electrode coupled to the first node;

a second transistor between the output terminal and the fourth input terminal, the second transistor having a gate electrode coupled to the second node;

a first capacitor between the first node and the fifth input terminal; and

a second capacitor between the second node and the output terminal.

3. The stage of claim 1, wherein the second driver comprises:

a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second input terminal; and

a seventh transistor between the second node and a first power source, the seventh transistor having a gate electrode coupled to the fifth input terminal.

4. The stage of claim 3, wherein the first power source is set to a gate-off voltage.

5. The stage of claim 3, wherein each of the sixth and seventh transistors comprises a plurality of transistors coupled in series.

6. The stage of claim 1, wherein the first driver comprises: a third transistor between the first input terminal and the second node, the third transistor having a gate electrode coupled to a third input terminal;

a fourth transistor between the fourth input terminal and the first node, the fourth transistor having a gate electrode coupled to the third input terminal; and

a fifth transistor between the fourth transistor and the first node, the fifth transistor having a gate electrode coupled to the first input terminal.

7. The stage of claim 6, wherein each of the third and fourth transistors comprises a plurality of transistors coupled in series.

8. The stage of claim 1, wherein the first driver comprises: a third transistor between the first input terminal and the second node, the third transistor having a gate electrode coupled to a third input terminal; and

a fourth transistor between the second input terminal and the first node, the fourth transistor having a gate electrode coupled to the second node.

9. An organic light emitting display device, comprising: pixels in an area defined by scan lines and data lines;

a data driver configured to supply data signals to the data lines; and

a scan driver comprising stages respectively coupled to the scan lines so as to supply scan signals to the scan lines, wherein odd-numbered stages are configured to be driven by first signals and a control signal, and even-numbered stages are configured to be driven by second signals and the control signal.

10. The organic light emitting display device of claim **9**, wherein each of the stages comprises:

- a first input terminal configured to receive a start signal or an output signal of a previous stage;
- second, third, and fourth input terminals configured to receive the first or second signals;
- a fifth input terminal configured to receive the control signal; and
- an output terminal configured to output a corresponding one of the scan signals.

11. The organic light emitting display device of claim **10**, wherein the first input terminal of each of a first stage and a second stage of the stages is configured to receive the start signal.

12. The organic light emitting display device of claim **11**, wherein the first input terminal of an odd-numbered stage of the stages is configured to receive an output signal of a previous odd-numbered stage of the stages, and

- wherein the first input terminal of an even-numbered stage of the stages is configured to receive an output signal of a previous even-numbered stage of the stages.

13. The organic light emitting display device of claim **10**, wherein each of the first and second signals comprises first, second, third, and fourth clock signals, and

- wherein the first to fourth clock signals are progressively supplied so that the voltage of the first to fourth clock signals are not overlapped at a low level with one another.

14. The organic light emitting display device of claim **13**, wherein a k-th (k is 1, 2, 3, or 4) clock signal of the second signals has a low level voltage that is overlapped with a low level voltage of a k-th clock signal of the first signals during at least one period.

15. The organic light emitting display device of claim **13**, wherein the second, third, and fourth input terminals of an i-th (i is 1, 9, or a multiple of 9) stage and an (i+1)-th stage are configured to receive the fourth, first, and second clock signals, respectively,

- wherein the second, third, and fourth input terminals of an (i+2)-th stage and an (i+3)-th stage are configured to receive the first, second, and third clock signals, respectively,

- wherein the second, third and fourth input terminals of an (i+4)-th stage and an (i+5)-th stage are configured to receive the second, third, and fourth clock signals, respectively, and

- wherein the second, third and fourth input terminals of an (i+6)-th stage and an (i+7)-th stage are configured to receive the third, fourth, and first clock signals, respectively.

16. The organic light emitting display device of claim **10**, wherein each stage comprises:

- an output unit configured to supply a corresponding one of the scan signals to the output terminal, according to voltages of first and second nodes; and
- first and second drivers configured to control the voltages of the first and second nodes.

17. The organic light emitting display device of claim **16**, wherein the output unit comprises:

- a first transistor between the fifth input terminal and the output terminal, the first transistor having a gate electrode coupled to the first node;
- a second transistor between the output terminal and the fourth input terminal, the second transistor having a gate electrode coupled to the second node;
- a first capacitor between the first node and the fifth input terminal; and
- a second capacitor between the second node and the output terminal.

18. The organic light emitting display device of claim **16**, wherein the first driver comprises:

- a third transistor between the first input terminal and the second node, the third transistor having a gate electrode coupled to a third input terminal;
- a fourth transistor between the fourth input terminal and the first node, the fourth transistor having a gate electrode coupled to the third input terminal; and
- a fifth transistor between the fourth transistor and the first node, the fifth transistor having a gate electrode coupled to the first input terminal.

19. The organic light emitting display device of claim **18**, wherein the start signal or the output signal of the previous stage, supplied to the first input terminal, is overlapped with a clock signal supplied to the third input terminal.

20. The organic light emitting display device of claim **16**, wherein the first driver comprises:

- a third transistor between the first input terminal and the second node, the third transistor having a gate electrode coupled to the third input terminal; and
- a fourth transistor between the second input terminal and the first node, the fourth transistor having a gate electrode coupled to the second node.

21. The organic light emitting display device of claim **20**, wherein the start signal or the output signal of the previous stage, supplied to the first input terminal, is overlapped with a clock signal supplied to the third input terminal.

22. The organic light emitting display device of claim **16**, wherein the second driver comprises:

- a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second input terminal;
- a seventh transistor between the second node and a first power source, the seventh transistor having a gate electrode coupled to the fifth input terminal; and
- eighth and ninth transistors coupled in series between the output terminal and the second node, wherein a gate electrode of the eighth transistor is coupled to the first node, and a gate electrode of the ninth transistor is coupled to the fourth input terminal.

23. The organic light emitting display device of claim **22**, wherein the first power source is set to a gate-off voltage.

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摘要(译)

一级包括输出单元，用于根据第一和第二节点的电压向输出端提供扫描信号；第一驱动器，被配置为控制第一和第二节点的电压，使得当前一级的开始信号或输出信号被提供给第一输入端时，从输出单元提供扫描信号；第二驱动器，被配置为控制第一和第二节点的电压，对应于提供给第二输入端子，第四输入端子和第五输入端子的信号，其中第二驱动器包括串联耦合的第八和第九晶体管。输出端子和第二节点，并且其中第八晶体管的栅极连接到第一节点，第九晶体管的栅极连接到第四输入端子。

